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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/347,106	07/02/1999	STANLEY A. HRONIK	M-7086US	3360

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SKJERVEN MORRILL LLP
25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110

EXAMINER
ANDERSON, MATTHEW D

ART UNIT	PAPER NUMBER
2186	7

DATE MAILED: 06/21/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/347,106	Hronik
Examiner	**Group Art Unit**
Matthew D. Anderson	2186

☒ Responsive to communication(s) filed on 5/21/02

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-56* is/are pending in the applicat

Of the above, claim(s) *56* is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-13, 17, 25, 27-36, and 46-55* is/are rejected.

☒ Claim(s) *14-16, 18-24, 26, and 37-45* is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *2-3*

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Drawings

1. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Response to Amendment

2. In response to the amendment filed 5/21/02: the specification has been amended.

Election/Restriction

3. Claim 56 is withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election of Group I, claims 1-55, was made without traverse in Paper No. 6.

Allowable Subject Matter

4. Claims 14-16, 18-24, 26, and 37-45 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: the prior art does not teach or suggest the following:

[Claim 14]: at least two registers for providing both a burst address received at the address bus and at least one read/write control signal received at the input terminal of the memory circuit to the at least two memory blocks sequentially in one clock cycle;

[Claim 18]: selecting a first write burst address stored in a first register corresponding to the last write burst operation;

[Claim 20 & 38]: the third write data item is written to one of the memory blocks at the initiation of the first write burst operations, and the fourth write data item is written to the other one of the memory blocks half a clock cycle after the initiation of the first write burst operation;

[Claims 26 & 37]: generating an echo clock signal when a read data item is provided on the data bus.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

7. Since allowable subject matter has been indicated, applicant is encouraged to submit formal drawings in response to this Office action. The early submission of formal drawings will permit the Office to review the drawings for acceptability and to resolve any informalities remaining therein before the application is passed to issue. This will avoid possible delays in the issue process.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-4, 10-13, 17, 25, 27-31, and 46-54 are rejected under 35 U.S.C. 102(b) as being anticipated by Ryan (US Patent # 5,749,086).

10. With respect to claims 1, 28, 46, 48, 50, 52, 54, Ryan discloses:

an address bus for receiving an address, as shown in item 105 of figure 3;

at least two memory blocks, as shown by the memory array 101 in figure 3;

an data bus for receiving data, as shown in item 130 of figure 3;

a sequential write burst and sequential read burst via the data bus, as shown in figure 19.

11. With respect to claims 2, 10, 29, 46, 49, Ryan discloses:

the first and second write data items are provided on the data bus at least one clock cycle after the first write burst operation is initiated, by teaching in figure 15, idle states (NOP) occurring after the write mode is selected, but before the write burst is started;

the first and second read data items are provided on the data bus at least one clock cycle after the first read burst operation is initiated, by teaching in figure 7, idle states (NOP) occurring after the read mode is selected, but before the read burst is started.

12. With respect to claims 3, 30, 48, 52, Ryan discloses a read/write control signal for indicating a write burst or a read burst operation, by teaching in Table 1 of column 6, lines 35-40, determining the mode by the command signals.

13. With respect to claims 4, 31, Ryan discloses second and third read or write bursts, as shown in figure 19.

14. With respect to claim 11, Ryan discloses an output circuit enable, by teaching in figure 19 of an output enable signal.

15. With respect to claim 12, Ryan discloses:

an input terminal for receiving the control signals, by showing the command decode device (104) in figure 3;

the output circuit being enabled by a 3-state signal, by teaching in Table 2 of column 6, lines 50-60, determining the read and write modes by the command signals.

16. With respect to claims 13, 47, 51, Ryan discloses a multiplexer for receiving a clock signal and read data items, and sequentially transferring to an output bus of the multiplexer, the read data items in accordance with the state of the clock signal, as shown in figures 3 and 19.

17. With respect to claims 25, 53, Ryan discloses a SRAM, in column 11, line 20.

18. With respect to claim 27, Ryan discloses:

a data-in bus for receiving write data items, as shown by the bus connected to the data-in buffer (126) of figure 3;

a data-out bus for providing read data items, as shown by the bus connected to the data-out buffer (128) of figure 3.

19. With respect to claim 54, Ryan discloses that consecutive read and write burst operations are capable to be performed sequentially in any order, by teaching in figure 11 of a burst read followed by a write, and in figure 19, of a burst write followed by a read.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 5-9, 32-36, and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryan and Hayes *et al.* (US Patent # 5,987,570).

22. Ryan teaches all other limitations of the parent claims, but does not specifically disclose the following:

23. With respect to claims 5, 32, 55, Hayes *et al.* disclose overlapping of the transfer of data items during half a clock cycle, by teaching in column 5, lines 12-15, overlapping of the first and second read block transactions.

24. With respect to claims 6-7, 17, 33-34, Hayes *et al.* disclose overlapping of write bursts, by teaching in column 14, lines 4-5, overlapping a write to physical memory with another burst.

25. With respect to claims 8-9, 35-36, Hayes *et al.* disclose overlapping of read bursts, by teaching in column 5, lines 12-15, overlapping of the first and second read block transactions.

26. It would have been obvious to one of ordinary skill in the art, having the teachings of Ryan and Hayes *et al.* before him at the time the invention was made, to modify the memory system with read and write bursts of Ryan to include overlapping of memory read/writes, as in

the memory access control system of Hayes *et al.*, in order to improve system throughput, as taught by Hayes *et al.*.

Conclusion

27. The prior art made of record on form PTO-892 and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to consider these references fully when responding to this action. The documents cited therein teach similar memory burst transmission systems.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Anderson whose telephone number is (703) 306-5931. The examiner can normally be reached on Monday-Friday, 2nd Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Matthew D. Anderson
June 13, 2002

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100